



Image AF/2815

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
BUR919990304US1

In Re Application Of: Ference et al.

Serial No.
09/732,240

Filing Date
12/07/2000

Examiner
Chris C. Chu

Group Art Unit
2815

Invention: MULTI-CHIP STACK AND METHOD OF FABRICATION UTILIZING SELF-ALIGNING
ELECTRICAL CONTACT ARRAY

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Signature

Dated: January 09, 2004

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cc:



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants: Ference et al.

Confirmation No.: 9501

Serial No.: 09/732,240

Group Art Unit: 2815

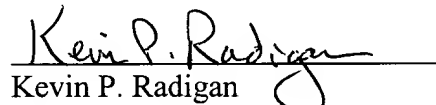
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Title: MULTI-CHIP STACK AND METHOD OF FABRICATION UTILIZING
SELF-ALIGNING ELECTRICAL CONTACT ARRAY

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Mail Stop Appeal Briefs - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 09, 2004.


Kevin P. Radigan
Attorney for Appellants
Registration No.: 31,789

Date of Signature: January 09, 2004.

To: Mail Stop Appeal Briefs - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Brief of Appellants

Dear Sir:

This is an appeal from a final rejection, dated October 2, 2003, rejecting claims 1-7, 10-14 & 30-35, all the claims being considered in the above-identified application. This Brief is accompanied by a transmittal letter authorizing the charging of appellants' deposit account for payment of the requisite fee set forth in 37 C.F.R. §1.17(c).

01/14/2004 AWONDAF1 00000115 090456 09732240

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Real Party In Interest

This application is assigned to **International Business Machines Corporation** by virtue of an assignment executed by the co-inventors on December 4, 2000 and December 7, 2000, and recorded with the United States Patent and Trademark Office at reel 011409, frame 0058, on December 7, 2000. Therefore, the real party in interest is **International Business Machines Corporation**.

Related Appeals and Interferences

To the knowledge of the appellants, appellants' undersigned legal representative, and the assignee, there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the instant appeal.

Status of Claims

This patent application was filed on December 7, 2000 with the United States Patent and Trademark Office. As filed, the application included twenty-nine (29) claims, of which two (2) were independent claims (i.e., claims 1 & 15).

In an initial communication from the Patent Office dated February 20, 2002 restriction was required under 35 U.S.C. §121 to either: claims 1-14 drawn to a structure, or claims 15-29, drawn to a method of joining. In appellants' response filed by facsimile transmission on March 18, 2002, appellants elected the subject matter of group I claims 1-14, with traverse.

In a first substantive Office Action, the restriction requirement was deemed proper and made final, and claims 1-14 were rejected under 35 U.S.C. §112, second paragraph, due to the presence of the term "substantially lower" in appellants' claim 1. Additionally, claims 1-10 were rejected under 35 U.S.C. §102(b) as being anticipated by Dalal et al. (U.S. Patent No. 5,796,591), and claims 1 & 11-14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Degani et al. (U.S. Patent No. 5,646,828) in view of Ikegami (U.S. Patent

No. 6,137,184). In appellant's response dated July 9, 2002, non-elected claims 15-29 were cancelled without prejudice, and new claims 30-33 were added.

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Appellants' received an Advisory Action dated January 22, 2003, which indicated that appellants' response to the final Office Action did not place the application in condition for allowance and would not be entered for purposes of appeal.

In a telephonic interview between the Examiner and appellants' representative conducted on January 23, 2003, the 35 U.S.C. §112, second paragraph, rejection to claim 1 was discussed. Based upon this discussion, appellants submitted a Request for Continued Examination and a Supplemental Response to Office Action on January 23, 2003, wherein claim 1 was amended to address the 35 U.S.C. §112, second paragraph, rejection. Substantively, appellants' supplemental response requested that the remarks contained in appellants' amendment dated January 13, 2003, responsive to the final Office Action be entered and considered.

In an Office Action dated April 8, 2003, claims 1-13 & 31-33 (and presumably claim 30) were rejected under 35 U.S.C. §103(a) as being unpatentable over Ju et al. (U.S. Patent No. 5,497,258) in view of Dalal et al. (U.S. Patent No. 5,796,591), while claim 14 was rejected under 35 U.S.C. §103(a) as being unpatentable over Ju et al. and Dalal et al. and in further view of Degani et al. (U.S. Patent No. 5,646,828). In appellants' response dated July

8, 2003, claim 1 was amended, claims 8 & 9 were cancelled without prejudice, and new claims 34 & 35 were added.

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A Notice of Appeal to the Board of Patent Appeals and Interferences was filed on December 2, 2003. The status of the claims is therefore as follows:

Claims allowed – none;

Claims objected to – none;

Claims rejected – 1-7, 10-14, & 30-35; and

Claims canceled – 8, 9, & 15-29.

Appellants are appealing the rejection of claims 1-7, 10-14, & 30-35.

Status of Amendments

The claims as set forth in the Appendix include all prior entered claim amendments.

Summary of Invention

Current solder bump array deposition technologies require an expensive and time-consuming mask alignment process. This alignment process becomes increasingly difficult and costly as the solder bump size and pitch is decreased. To realize the full advantages of multi-chip stack technology, very high solder bump interconnection density is needed. Unfortunately, the multi-chip stack structure may suffer the expensive and inherent technology limitations associated with current solder bump array technologies. The present invention is designed to address these inherent limitations by providing a self-aligning interconnect structure.

Appellants recite a structure which includes a first substrate (10, 100) and a second substrate (200) and first solder bumps (14, 114, 214) and second solder bumps (12, 112, 212) offset therebetween. The second solder bumps are for aligning the first substrate and second substrate before melting of the first solder bumps. The first solder bumps and the second solder bumps are separate sets of solder bumps disposed between the first substrate and the second substrate. The second solder bumps have at least a portion that melt at a lower temperature than the first solder bumps.

In an enhanced aspect, the recited structure is further characterized by the second solder bumps (12, 112, 212) having a portion with a higher concentration of tin than the first solder bumps (14, 114, 214), wherein the portion is the entire second solder bumps. (e.g., claim 7).

In a further aspect, the structure is characterized by the second solder bumps melting at a temperature at least 25°C less than the first solder bumps (e.g., specification, page 13, lines 19-29, and claims 10 & 32). In still another aspect, the structure is characterized by the second solder bumps having uniform composition and melting at a lower temperature than the first solder bumps (e.g., claims 34 & 35).

Issues

1. Whether claims 1-7, 10-13, & 30-35 were obvious under 35 U.S.C. §103(a) over Ju et al. in view of Dalal et al.
2. Whether claim 14 was obvious over Ju et al. and Dalal et al. as applied to claims 1 & 11, and further in view of Degani et al.

Grouping of Claims

Since each ground of rejection provides a grouping of claims, the following groups of claims are included herein:

- I. Claims 1-7, 10-13, & 30-35.
- II. Claim 14.

Appellants respectfully submit that the claims of Group I do not fall to stand or fall together. For example, claims 7, 10, 32, 34 & 35 are each believed to include additional features that provide a separate basis for patentability.

Argument

Group I: Claims 1-7, 10-13, & 30-35

As noted, claims 1-7, 10-13, & 30-35 stand rejected as obvious over Ju et al. in view of Dalal et al. Reversal of this rejection is respectfully requested.

Initially, appellants respectfully traverse the combination of Ju et al. and Dalal et al. to the extent that it is alleged that the combination suggests their claimed invention. The justification given for the combination is to “increase the yield and have a joint that has high reliability as taught by Dalal et al. in column 4, lines 53 and 54.” Appellants respectfully submit that this justification does not identify an adequate teaching, suggestion or incentive in the art to combine these references in the manner set forth in the final Office Action. For example, there is no justification given in the record or cited in the art itself why one skilled in the art would selectively apply the extrapolated teachings of Dalal et al. to only one set of solder bumps depicted by Ju et al.

Appellants respectfully submit that the only suggestion or incentive for combining the two teachings in the manner set forth in the final Office Action is presented in appellants’ own disclosure, which as well known, cannot be used as a reference against their claimed invention. In this case, the basis for selective combination of Dalal et al. with one set of solder bumps in Ju et al. is believed drawn from appellants own disclosure, in violation of this principle.

Moreover, neither Ju et al. nor Dalal et al. discuss the problem addressed by the present invention, i.e., how to achieve better alignment of fine pitched solder bumps. As cited in the final Office Action, Dalal et al. is addressing increasing yield and having a joint with higher reliability. This is achieved in Dalal et al. by providing solder bumps 38 with tin caps 41 to achieve better connection to copper pads 20.

Assuming, arguendo, that the combination set forth in the final Office Action is proper, appellants respectfully submit that the combination still fails to teach or suggest features of their claimed invention. For example, the independent claims recite first solder bumps and second solder bumps offset between, for example, the first substrate and the second substrate (see claim 1). These first solder bumps and second solder bumps are separate solder bumps disposed between the first substrate and the second substrate. The second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps. Further, appellants independent claims recite that the second set of solder bumps are for aligning the first substrate and the second substrate before melting the first solder bumps. This structure and function are very different from the teachings of Ju et al. and Dalal et al., either alone or in combination.

Ju et al. teach a structure having a first set of solder bumps (25 or 36/25) and a second set of solder bumps (26 or 36/26) offset between a first and second substrate. A careful reading of Ju et al. fails to uncover any teaching, suggestion or implication that the different sets of solder bumps have different melting temperatures. For an alleged teaching of this concept, the Office Action relies upon Dalal et al.

Dalal et al. describe a direct chip attached circuit card wherein an IC chip 30 includes a solder bump 38 with a cap of low melting point metal 41 (e.g., tin). Solder bump 38 aligns over and connects to a copper pad 20 disposed above a laminate 10. The final Office Action characterizes Dalal et al. as disclosing in FIG. 5, and column 8, lines 48-51, bumps (38) having at least a portion (41) that melt at a lower temperature than other bumps (20). This characterization of the teachings of Dalal et al. is respectfully traversed to the extent deemed applicable to appellants' recited structure.

Appellants' independent claims (i.e., claims 1 & 30) expressly recite first solder bumps and second solder bumps wherein the second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps. The copper pad 20 in Dalal et al. is simply adjoining metallurgy to which the solder bump 38 is to be connected. One skilled in the art would not read the teachings thereof as somehow suggesting that copper pad 20 is a "solder bump". The phrase "solder bump" refers to a particular metallurgy, which is distinct

from copper pads or copper lines on the adjoining structure. Thermal cycling is employed to melt a solder bump and electrically interconnect two structures. Copper pads do not melt during this thermal cycling. In fact, it would be impossible in Dalal et al. to melt the copper pads 20, since the organic laminate on which the pads are disposed would be destroyed as well as any other copper lines which may be present. Thus, appellants respectfully traverse the characterization of copper pad 20 as a “bump” functionally equivalent to appellants’ recited solder bump structure. Appellants’ application is directed to a structure having “first solder bumps and second solder bumps”. Because of this, appellants respectfully submit that one of ordinary skill in the art would not have read the teachings of Dalal et al. as being applicable to their recited solder bumps. Since in Dalal et al., the “bump” comprising copper pad 20 is a completely different metallurgy and does not melt in order to electrically interconnect two structures.

In addition, a careful reading of Ju et al. and Dalal et al. also fails to uncover any teaching, suggestion or implication of two different types of solder bumps, with one type of solder bumps having a melting temperature that is different from the other type of solder bumps. If Dalal et al. were to be combined with Ju et al. then one of ordinary skill in the art would combine the solder bump cap presented therein with all the solder bumps (25 or 35/25) and (26 or 36/26), and not just one set of solder bumps as suggested in the final Office Action. In Dalal et al., all solder bumps are of a composite solder bump structure. The “bumps” comprising copper pad 20 simply do not comprise “solder bumps”, and appellants respectfully submit that there is no suggestion in the applied art to use the teachings of Dalal et al. on only one set of solder bumps, and not the other set of solder bumps in Ju et al.

Still further, neither Ju et al. nor Dalal et al. are differentiating between different solder bumps and applying a different melting temperature to the first solder bumps and the second solder bumps to achieve enhanced alignment as recited by appellants in the independent claims presented. For example, appellants’ structure recited in claim 1 is further characterized by the second solder bumps being for aligning the first substrate and the second substrate before melting the first solder bumps. A careful reading of Ju et al. fails to uncover any teaching, suggestion or implication of this concept. The alignment reflow discussed by

Ju et al. occurs concurrently across all solder joints. There is no differentiation in Ju et al. between the first solder bumps and the second solder bumps as having different melting temperatures, nor of such a concept being used to facilitate alignment of a first substrate and a second substrate. Appellants' independent claims specifically recite functionality which states that the second solder bumps accomplish this alignment before melting the first solder bumps. The term "melting" means that the solder bumps become altered from a solid to a liquid phase. Thus, in appellants' claimed invention, the second solder bumps have at least a portion that melts at a lower temperature, and this facilitates alignment of the first substrate and the second substrate before the first solder bumps ever melt. In Ju et al, both sets of solder bumps would necessarily melt at the same time since both have the same composition.

In view of the differences noted above, appellants respectfully submit that their invention as recited in independent claims 1 & 30 would not have been obvious to one of ordinary skill in the art based upon the structures of Ju et al. and Dalal et al. Therefore, reversal of the obviousness as rejection to these claims is respectfully requested.

The dependent claims are believed patentable for the same reasons as the independent claims from which they directly or ultimately depend, as well as for their own additional characterizations.

For example, claim 7 recites the structure of claims 1 and 3 where the second solder bumps have, across the entire solder bumps, a higher concentration of tin than the first solder bumps. Dalal et al. disclose in FIG. 5, and column 8, lines 49-57, that the cap 41 is a low melting point cap that surrounds a solder bump 38. This cap clearly does not relate to the concentration of the solder bump itself, and is distinct from appellants' recited structure wherein the entire second solder bumps comprise a higher concentration of tin than the first solder bumps. Appellants claim 34 & 35 further characterize the structure of claims 1 & 30, respectively, by indicating that the second solder bumps have a uniform composition and melt at a lower temperature than the first set of solder bumps. This uniform composition of the solder bumps is clearly distinct from the teachings of Dalal et al. wherein solder bump 38 has a cap 41. The structure described by Dalal et al. is simply not a solder bump of uniform composition and which has a lower melting temperature than another set of solder bumps.

Cap 41 and solder bump 38 clearly comprise structures of different composition in Dalal et al. The final Office Action provides no indication as to how the teachings of Dalal et al. could be combined with Ju et al. to obtain appellants' recited concept of uniform composition in the second solder bump.

Claims 10 & 32, further state that the second solder bumps melt at a temperature at least 25°C less than the first solder bumps. This claim provides a further characterization on appellants' solder bumps melting at a "lower temperature" than the first solder bumps. A careful review of FIG. 5, and column 8, lines 48-57 of Dalal et al. (cited in the final Office Action), fails to uncover any relevant discussion to the claimed subject matter. The final Office Action characterizes copper pad 20 in Dalal et al. as somehow comprising a second type of solder bumps as recited by appellants. This characterization is believed erroneous. Copper pads represent a completely different metallurgy than solder bumps and they are not relevant to appellants' claimed subject matter. The characterization "solder" is a well known metallurgy to those skilled in the art, and copper does not comprise solder as the term is understood.

For the above reasons, appellants respectfully request reversal of the obvious rejection to all claims of Group I.

Group II – Claim 14

Claim 14 stands rejected as obvious over Ju et al. and Dalal et al. as applied against claims 1 & 11, and further in view of Degani et al. Reversal of this rejection is respectfully requested.

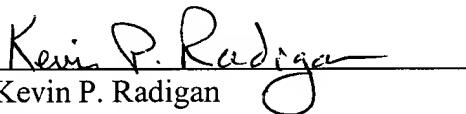
The final Office Action notes that the combination of Ju et al. and Dalal et al. does not disclose that the second semiconductor chip further comprises wire bond pads for bonding to a printed circuit board. For a teaching of this concept, the Office Action relies upon Degani et al. Without acquiescing to the characterizations of Degani et al. contained in the final Office Action, appellants respectfully submit that Degani et al. provides no teaching, suggestion, or implication relevant to the above-noted deficiencies of Ju et al. and Dalal et al.

when applied against the independent claims presented. For this reason, appellants respectfully request reversal of the obviousness rejection to claim 14 of Group II.

Conclusion

Appellants respectfully request reversal of the rejections as set forth in the final Office Action. Appellants submit that their claimed invention would not have been rendered obvious by Ju et al., Dalal et al. and/or Degani et al. These patents do not individually or in combination teach, suggest, or imply appellants' recited structure which includes, for example, first solder bumps and second solder bumps offset between a first substrate and a second substrate, wherein the second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps, and wherein the second solder bumps are for aligning the first substrate and the second substrate before melting of the first solder bumps.

For all of the above reasons, appellants allege error in rejecting their claims as obvious based on Ju et al. and Dalal et al., or Ju et al., Dalal et al. and Degani et al. Accordingly, reversal of the rejections is respectfully requested.


Kevin P. Radigan
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Registration No.: 31,789

Dated: January 09, 2004.

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Appendix

1. A structure comprising:

a first substrate and a second substrate; and

first solder bumps and second solder bumps offset therebetween, wherein said first solder bumps and said second solder bumps are separate solder bumps disposed between said first substrate and said second substrate, and wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps; and

wherein said second solder bumps are for aligning said first substrate and said second substrate before melting said first solder bumps.

2. A structure as recited in claim 1, wherein said second solder bumps are larger than said first solder bumps.

3. A structure as recited in claim 1, wherein said second solder bumps comprise a portion having a higher concentration of tin than does said first solder bumps.

4. A structure as recited in claim 3, wherein said portion comprises a eutectic concentration of tin.

5. A structure as recited in claim 3, wherein said portion is adjacent to said second substrate.

6. A structure as recited in claim 3, wherein said portion is centrally located within said second solder bump.

7. A structure as recited in claim 3, wherein said portion is said entire second solder bumps.

10. A structure as recited in claim 1, wherein said second solder bumps melt at a temperature at least 25C less than said first solder bumps.

11. A structure as recited in claim 1, wherein said first substrate comprises a first semiconductor chip.

12. A structure as recited in claim 11, wherein said second substrate comprises a second semiconductor chip.

13. A structure as recited in claim 12, wherein said second chip is larger than said first chip.

14. A structure as recited in claim 12, wherein said second chip further comprises wire bond pads for bonding to a printed circuit board.

30. A structure comprising:

a first substrate having a main surface with first solder bumps and second solder bumps separately disposed thereacross; and

wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps, said second solder bumps being for aligning said first substrate to a second substrate before melting said first solder bumps.

31. The structure of claim 30, wherein said second solder bumps are larger than said first solder bumps.

32. The structure of claim 30, wherein said second solder bumps melt at a temperature at least 25°C less than said first solder bumps.

33. The structure of claim 32, wherein the first substrate comprises a semiconductor chip.

34. The structure of claim 1, wherein said second solder bumps have a uniform composition and melt at a lower temperature than said first solder bumps.

35. The structure of claim 30, wherein said second solder bumps have a uniform composition and melt at a lower temperature than said first solder bumps.

* * * * *



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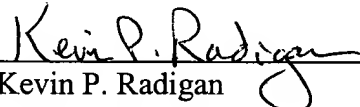
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Brief of Appellants

Dear Sir:

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Summary of Invention

Current solder bump array deposition technologies require an expensive and time-consuming mask alignment process. This alignment process becomes increasingly difficult and costly as the solder bump size and pitch is decreased. To realize the full advantages of multi-chip stack technology, very high solder bump interconnection density is needed. Unfortunately, the multi-chip stack structure may suffer the expensive and inherent technology limitations associated with current solder bump array technologies. The present invention is designed to address these inherent limitations by providing a self-aligning interconnect structure.

Appellants recite a structure which includes a first substrate (10, 100) and a second substrate (200) and first solder bumps (14, 114, 214) and second solder bumps (12, 112, 212) offset therebetween. The second solder bumps are for aligning the first substrate and second substrate before melting of the first solder bumps. The first solder bumps and the second solder bumps are separate sets of solder bumps disposed between the first substrate and the second substrate. The second solder bumps have at least a portion that melt at a lower temperature than the first solder bumps.

In an enhanced aspect, the recited structure is further characterized by the second solder bumps (12, 112, 212) having a portion with a higher concentration of tin than the first solder bumps (14, 114, 214), wherein the portion is the entire second solder bumps. (e.g., claim 7).

In a further aspect, the structure is characterized by the second solder bumps melting at a temperature at least 25°C less than the first solder bumps (e.g., specification, page 13, lines 19-29, and claims 10 & 32). In still another aspect, the structure is characterized by the second solder bumps having uniform composition and melting at a lower temperature than the first solder bumps (e.g., claims 34 & 35).

Issues

1. Whether claims 1-7, 10-13, & 30-35 were obvious under 35 U.S.C. §103(a) over Ju et al. in view of Dalal et al.
2. Whether claim 14 was obvious over Ju et al. and Dalal et al. as applied to claims 1 & 11, and further in view of Degani et al.

Grouping of Claims

Since each ground of rejection provides a grouping of claims, the following groups of claims are included herein:

- I. Claims 1-7, 10-13, & 30-35.
- II. Claim 14.

Appellants respectfully submit that the claims of Group I do not fall to stand or fall together. For example, claims 7, 10, 32, 34 & 35 are each believed to include additional features that provide a separate basis for patentability.

Argument

Group I: Claims 1-7, 10-13, & 30-35

As noted, claims 1-7, 10-13, & 30-35 stand rejected as obvious over Ju et al. in view of Dalal et al. Reversal of this rejection is respectfully requested.

Initially, appellants respectfully traverse the combination of Ju et al. and Dalal et al. to the extent that it is alleged that the combination suggests their claimed invention. The justification given for the combination is to “increase the yield and have a joint that has high reliability as taught by Dalal et al. in column 4, lines 53 and 54.” Appellants respectfully submit that this justification does not identify an adequate teaching, suggestion or incentive in the art to combine these references in the manner set forth in the final Office Action. For example, there is no justification given in the record or cited in the art itself why one skilled in the art would selectively apply the extrapolated teachings of Dalal et al. to only one set of solder bumps depicted by Ju et al.

Appellants respectfully submit that the only suggestion or incentive for combining the two teachings in the manner set forth in the final Office Action is presented in appellants’ own disclosure, which as well known, cannot be used as a reference against their claimed invention. In this case, the basis for selective combination of Dalal et al. with one set of solder bumps in Ju et al. is believed drawn from appellants own disclosure, in violation of this principle.

Moreover, neither Ju et al. nor Dalal et al. discuss the problem addressed by the present invention, i.e., how to achieve better alignment of fine pitched solder bumps. As cited in the final Office Action, Dalal et al. is addressing increasing yield and having a joint with higher reliability. This is achieved in Dalal et al. by providing solder bumps 38 with tin caps 41 to achieve better connection to copper pads 20.

Assuming, arguendo, that the combination set forth in the final Office Action is proper, appellants respectfully submit that the combination still fails to teach or suggest features of their claimed invention. For example, the independent claims recite first solder bumps and second solder bumps offset between, for example, the first substrate and the second substrate (see claim 1). These first solder bumps and second solder bumps are separate solder bumps disposed between the first substrate and the second substrate. The second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps. Further, appellants independent claims recite that the second set of solder bumps are for aligning the first substrate and the second substrate before melting the first solder bumps. This structure and function are very different from the teachings of Ju et al. and Dalal et al., either alone or in combination.

Ju et al. teach a structure having a first set of solder bumps (25 or 36/25) and a second set of solder bumps (26 or 36/26) offset between a first and second substrate. A careful reading of Ju et al. fails to uncover any teaching, suggestion or implication that the different sets of solder bumps have different melting temperatures. For an alleged teaching of this concept, the Office Action relies upon Dalal et al.

Dalal et al. describe a direct chip attached circuit card wherein an IC chip 30 includes a solder bump 38 with a cap of low melting point metal 41 (e.g., tin). Solder bump 38 aligns over and connects to a copper pad 20 disposed above a laminate 10. The final Office Action characterizes Dalal et al. as disclosing in FIG. 5, and column 8, lines 48-51, bumps (38) having at least a portion (41) that melt at a lower temperature than other bumps (20). This characterization of the teachings of Dalal et al. is respectfully traversed to the extent deemed applicable to appellants' recited structure.

Appellants' independent claims (i.e., claims 1 & 30) expressly recite first solder bumps and second solder bumps wherein the second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps. The copper pad 20 in Dalal et al. is simply adjoining metallurgy to which the solder bump 38 is to be connected. One skilled in the art would not read the teachings thereof as somehow suggesting that copper pad 20 is a "solder bump". The phrase "solder bump" refers to a particular metallurgy, which is distinct

from copper pads or copper lines on the adjoining structure. Thermal cycling is employed to melt a solder bump and electrically interconnect two structures. Copper pads do not melt during this thermal cycling. In fact, it would be impossible in Dalal et al. to melt the copper pads 20, since the organic laminate on which the pads are disposed would be destroyed as well as any other copper lines which may be present. Thus, appellants respectfully traverse the characterization of copper pad 20 as a “bump” functionally equivalent to appellants’ recited solder bump structure. Appellants’ application is directed to a structure having “first solder bumps and second solder bumps”. Because of this, appellants respectfully submit that one of ordinary skill in the art would not have read the teachings of Dalal et al. as being applicable to their recited solder bumps. Since in Dalal et al., the “bump” comprising copper pad 20 is a completely different metallurgy and does not melt in order to electrically interconnect two structures.

In addition, a careful reading of Ju et al. and Dalal et al. also fails to uncover any teaching, suggestion or implication of two different types of solder bumps, with one type of solder bumps having a melting temperature that is different from the other type of solder bumps. If Dalal et al. were to be combined with Ju et al. then one of ordinary skill in the art would combine the solder bump cap presented therein with all the solder bumps (25 or 35/25) and (26 or 36/26), and not just one set of solder bumps as suggested in the final Office Action. In Dalal et al., all solder bumps are of a composite solder bump structure. The “bumps” comprising copper pad 20 simply do not comprise “solder bumps”, and appellants respectfully submit that there is no suggestion in the applied art to use the teachings of Dalal et al. on only one set of solder bumps, and not the other set of solder bumps in Ju et al.

Still further, neither Ju et al. nor Dalal et al. are differentiating between different solder bumps and applying a different melting temperature to the first solder bumps and the second solder bumps to achieve enhanced alignment as recited by appellants in the independent claims presented. For example, appellants’ structure recited in claim 1 is further characterized by the second solder bumps being for aligning the first substrate and the second substrate before melting the first solder bumps. A careful reading of Ju et al. fails to uncover any teaching, suggestion or implication of this concept. The alignment reflow discussed by

Ju et al. occurs concurrently across all solder joints. There is no differentiation in Ju et al. between the first solder bumps and the second solder bumps as having different melting temperatures, nor of such a concept being used to facilitate alignment of a first substrate and a second substrate. Appellants' independent claims specifically recite functionality which states that the second solder bumps accomplish this alignment before melting the first solder bumps. The term "melting" means that the solder bumps become altered from a solid to a liquid phase. Thus, in appellants' claimed invention, the second solder bumps have at least a portion that melts at a lower temperature, and this facilitates alignment of the first substrate and the second substrate before the first solder bumps ever melt. In Ju et al, both sets of solder bumps would necessarily melt at the same time since both have the same composition.

In view of the differences noted above, appellants respectfully submit that their invention as recited in independent claims 1 & 30 would not have been obvious to one of ordinary skill in the art based upon the structures of Ju et al. and Dalal et al. Therefore, reversal of the obviousness as rejection to these claims is respectfully requested.

The dependent claims are believed patentable for the same reasons as the independent claims from which they directly or ultimately depend, as well as for their own additional characterizations.

For example, claim 7 recites the structure of claims 1 and 3 where the second solder bumps have, across the entire solder bumps, a higher concentration of tin than the first solder bumps. Dalal et al. disclose in FIG. 5, and column 8, lines 49-57, that the cap 41 is a low melting point cap that surrounds a solder bump 38. This cap clearly does not relate to the concentration of the solder bump itself, and is distinct from appellants' recited structure wherein the entire second solder bumps comprise a higher concentration of tin than the first solder bumps. Appellants claim 34 & 35 further characterize the structure of claims 1 & 30, respectively, by indicating that the second solder bumps have a uniform composition and melt at a lower temperature than the first set of solder bumps. This uniform composition of the solder bumps is clearly distinct from the teachings of Dalal et al. wherein solder bump 38 has a cap 41. The structure described by Dalal et al. is simply not a solder bump of uniform composition and which has a lower melting temperature than another set of solder bumps.

Cap 41 and solder bump 38 clearly comprise structures of different composition in Dalal et al. The final Office Action provides no indication as to how the teachings of Dalal et al. could be combined with Ju et al. to obtain appellants' recited concept of uniform composition in the second solder bump.

Claims 10 & 32, further state that the second solder bumps melt at a temperature at least 25°C less than the first solder bumps. This claim provides a further characterization on appellants' solder bumps melting at a "lower temperature" than the first solder bumps. A careful review of FIG. 5, and column 8, lines 48-57 of Dalal et al. (cited in the final Office Action), fails to uncover any relevant discussion to the claimed subject matter. The final Office Action characterizes copper pad 20 in Dalal et al. as somehow comprising a second type of solder bumps as recited by appellants. This characterization is believed erroneous. Copper pads represent a completely different metallurgy than solder bumps and they are not relevant to appellants' claimed subject matter. The characterization "solder" is a well known metallurgy to those skilled in the art, and copper does not comprise solder as the term is understood.

For the above reasons, appellants respectfully request reversal of the obvious rejection to all claims of Group I.

Group II – Claim 14

Claim 14 stands rejected as obvious over Ju et al. and Dalal et al. as applied against claims 1 & 11, and further in view of Degani et al. Reversal of this rejection is respectfully requested.

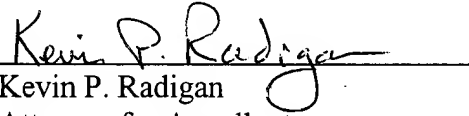
The final Office Action notes that the combination of Ju et al. and Dalal et al. does not disclose that the second semiconductor chip further comprises wire bond pads for bonding to a printed circuit board. For a teaching of this concept, the Office Action relies upon Degani et al. Without acquiescing to the characterizations of Degani et al. contained in the final Office Action, appellants respectfully submit that Degani et al. provides no teaching, suggestion, or implication relevant to the above-noted deficiencies of Ju et al. and Dalal et al.

when applied against the independent claims presented. For this reason, appellants respectfully request reversal of the obviousness rejection to claim 14 of Group II.

Conclusion

Appellants respectfully request reversal of the rejections as set forth in the final Office Action. Appellants submit that their claimed invention would not have been rendered obvious by Ju et al., Dalal et al. and/or Degani et al. These patents do not individually or in combination teach, suggest, or imply appellants' recited structure which includes, for example, first solder bumps and second solder bumps offset between a first substrate and a second substrate, wherein the second solder bumps have at least a portion that melts at a lower temperature than the first solder bumps, and wherein the second solder bumps are for aligning the first substrate and the second substrate before melting of the first solder bumps.

For all of the above reasons, appellants allege error in rejecting their claims as obvious based on Ju et al. and Dalal et al., or Ju et al., Dalal et al. and Degani et al. Accordingly, reversal of the rejections is respectfully requested.


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Appendix

1. A structure comprising:

a first substrate and a second substrate; and

first solder bumps and second solder bumps offset therebetween, wherein said first solder bumps and said second solder bumps are separate solder bumps disposed between said first substrate and said second substrate, and wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps; and

wherein said second solder bumps are for aligning said first substrate and said second substrate before melting said first solder bumps.
2. A structure as recited in claim 1, wherein said second solder bumps are larger than said first solder bumps.
3. A structure as recited in claim 1, wherein said second solder bumps comprise a portion having a higher concentration of tin than does said first solder bumps.
4. A structure as recited in claim 3, wherein said portion comprises a eutectic concentration of tin.
5. A structure as recited in claim 3, wherein said portion is adjacent to said second substrate.
6. A structure as recited in claim 3, wherein said portion is centrally located within said second solder bump.
7. A structure as recited in claim 3, wherein said portion is said entire second solder bumps.
10. A structure as recited in claim 1, wherein said second solder bumps melt at a temperature at least 25C less than said first solder bumps.

11. A structure as recited in claim 1, wherein said first substrate comprises a first semiconductor chip.

12. A structure as recited in claim 11, wherein said second substrate comprises a second semiconductor chip.

13. A structure as recited in claim 12, wherein said second chip is larger than said first chip.

14. A structure as recited in claim 12, wherein said second chip further comprises wire bond pads for bonding to a printed circuit board.

30. A structure comprising:

a first substrate having a main surface with first solder bumps and second solder bumps separately disposed thereacross; and

wherein said second solder bumps have at least a portion that melts at a lower temperature than said first solder bumps, said second solder bumps being for aligning said first substrate to a second substrate before melting said first solder bumps.

31. The structure of claim 30, wherein said second solder bumps are larger than said first solder bumps.

32. The structure of claim 30, wherein said second solder bumps melt at a temperature at least 25°C less than said first solder bumps.

33. The structure of claim 32, wherein the first substrate comprises a semiconductor chip.

34. The structure of claim 1, wherein said second solder bumps have a uniform composition and melt at a lower temperature than said first solder bumps.

35. The structure of claim 30, wherein said second solder bumps have a uniform composition and melt at a lower temperature than said first solder bumps.

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